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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
Bily WANG, Jonnie CHUANG, Chi-Wen HUNG Art unit: 2818

Serial No. 10/697,610 Examiner: HO, Tu Tu V

Filed: Oct. 31, 2003

For: IC PACKAGE WITH STACKED SHEET METAL SUBSTRATE

AMENDMENT

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In response to USPTO communication dated Sept.7, 2004, please amend the application as follows:

IN THE CLAIMS:

Claim 1. (currently amended) An integrated circuit (IC) package, comprising:

a first section and a second section of a common stacked metal substrate with an upper layer and a lower layer;

an IC chip having two electrodes each coupled to one of the two sections respectively; and

a glue to hold said first section and said second section together, leaving the far ends of said first section and said second section uncovered, [serving as said one terminal and said second terminal respectively] said far ends serving as terminals for the IC package.

Claim 2. (original) The IC package as described in claim 1, further comprising a second IC diode chip mounted at the bottom of said lower layer and connected in parallel with the IC diode chip mounted on the upper layer of said first section.

Claim 3. ((original) The IC package as described in claim 1, further comprising a through hole in each of said first section and said section for said glue to fill, thereby strengthening the hold of the glue to hold said first section and said second section.

Claim 4.(original) The IC package as described in claim 1, wherein said first section and said second section of said package are recessed, so that the glue covers only the recesses of the recessed section.

Claim 5.(original) The IC package as described in claim 1, wherein the gap between said first section and said second section is zigzag to increase the hold of the glue.

Claim 6. (original) The IC package as described in claim 1, wherein the coupling is wire-bonding.

Claim 7. (currently amended) The IC package as described in claim 1, wherein the coupling is by flip-chip technology.

Claim 8. (original) The IC package as described in claim 1, further comprising a matrix of said IC package mounted first on said common stacked metal substrate, and then cut apart in two orthogonal directions to yield individual packages.